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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,160	07/25/2001	Toshiharu Yanagida	09792909-5171	7228

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EXAMINER

IM, JUNGHWAM

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 04/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/915,160	Applicant(s) YANAGIDA, TOSHIHARU	
	Examiner Junghwa M. Im	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2,6 and 25-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2,6 and 25-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 5, 6, 25-26 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Milewski et al. (US 6,330,967), hereafter Milewski in view of Nishikawa et al. (US 5,878,943), hereafter Nishikawa.

Regarding claims 5, 6 and 25, Figure 4 of Milewski shows a semiconductor apparatus comprising:

- a semiconductor chip 10 inherently having a circuit pattern;
- a plurality of solder bumps 33 of two different materials 35 on the semiconductor chip connect to the circuit pattern, the solder bumps forming spaces;
- a passivation film 14 [in Fig. 3] disposed directly on the semiconductor chip and said solder bumps, said passivation film being disposed in the spaces between solder bumps such that upper surfaces of said solder bumps protrude from said resin layer;
- a eutectic solder layer 37 disposed on the upper surface of the solder ball;
- a mounting board 21;
- a plurality of lands 53 formed on said mounting board and aligned opposite said solder bumps;

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a precoated solder layer 51 disposed on said lands [a solder wettable layer with an oxidation inhibitor on the surface; col. 5, lines 1-5];

wherein said eutectic solder layer of said solder bumps and said precoated solder layer join said upper surfaces of said solder bumps to said lands of said mounting board such that a stacked structure is obtained [col. 5, lines 7-16];

wherein a gap is formed between said passivation layer and said mounting board of said stacked structure.

Milewski fail to disclose the aspect of cleaning the upper surface of the metal bumps. Figure 18 of Nishikawa shows the surfaces of the metal bumps being cleaned (col.12, lines 18-25). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Nishikawa to the device of Milewski in order to enhance the strength of the soldered junction through having a clean surface of metal bumps.

Even though Milewski does not explicitly disclose that the passivation layer is a resin film, it would be obvious to one of ordinary skill in the art at the time of the invention to use resin for the passivation layer of Milewski with the teachings of Nishikawa since resin is well known and widely used passivation/dielectric material for packaging the semiconductor device.

Regarding claim 2, Nishikawa teaches the surfaces of the metal bumps being cleaned of components causing a rise of a connection resistance and a drop in a joint strength at least connection interfaces. Nishikawa teaches, throughout the specification especially in col. 1, lines 22-40, cleaning method of oxide/contamination coating on the surface of metal bumps to enhance better alignment between the soldering joint.

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Regarding claim 26, Milewski discloses that said eutectic solder layer of said solder bumps and said precoated solder layer intermix to join said upper surfaces of said solder bumps to said lands of said mounting board (col. 3, lines 9-14).

Regarding claim 29, Milewski discloses said precoated solder layer comprises a eutectic solder. (col. 4, lines 53-56).

Regarding claim 30, Figure 4 of Milewski shows each of said lands 53 has a top side, a bottom side opposite said top side and directly contacting the mounting board 21, and it is inherent to form side walls extending from the topside to the bottom side to have a thickness.

Regarding claim 31, Figure 4 of Milewski shows the mounting board 21 includes an upper surface, the upper surface having land portions on which said lands 53 are formed.

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milewski and Nishikawa as applied to claim 25 above, and further in view of Celling (US 3,811,183).

Regarding claim 27, the combined teachings of Milewski and Nishikawa show substantially the entire claimed structure except "said resin film includes an epoxy-based resin film cured at about 150°C for about 5 hours after being spin-coated in place." Celling discloses that epoxy-based resin film is used for the passivation/resin layer. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Celling to the device of Milewski and Nishikawa in order to have the resin film included an epoxy-based resin film since an epoxy-based resin film is well-known and readily available passivation material.

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Also, note that “cured at about 150°C for about 5 hours after being spin-coated in place” is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milewski and Nishikawa as applied to claim 25 above, and further in view of Wang et al. (US 6,168,972), hereinafter Wang.

Regarding claim 28, the combined teachings of Milewski and Nishikawa show substantially the entire claimed structure except “said upper surfaces of said solder bumps are plasma cleaned of impurities.” Wang discloses that the upper surfaces of said solder bumps are plasma cleaned of impurities (col. 8, lines 29-35). It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Wang to the device of Milewski and Nishikawa in order to have the upper surfaces of said solder bumps are plasma cleaned of impurities to facilitate solder reflow.

Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Milewski and Nishikawa as applied to claim 31 above, and further in view of Oya (US 6,168,972).

Regarding claim 32, the combined teachings of Milewski and Nishikawa show substantially the entire claimed structure except “solder resists formed on the mounting board intermediate adjacent lands of the plurality of lands.”

Fig. 7 of Oya shows solder resists 13 formed on the mounting board intermediate adjacent lands of the plurality of lands. It would have been obvious to one of ordinary skill in

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the art at the time of the invention to incorporate the teachings of Oya to the device of Milewski and Nishikawa in order to have solder resists formed on the mounting board intermediate adjacent lands of the plurality of lands to improve the joint strength.

Response to Arguments

Applicant's arguments filed January 6, 2005 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant amended claims.

In addition, Examiner presents the remarks below in response to Applicant's arguments.

Applicant argues that "Milewski and Nishikawa, taken alone or in combination, do not disclose disposing a resin film directly on the semiconductor chip and the solder bumps or a plurality of lands formed on the mounting board, as claimed. Specifically, Milewski does not show or suggest disposing a resin film directly on the solder bumps," and in particular, "the layer 14 is not 'disposed directly on ...(the) solder bumps,' as claimed. Instead, the passivation layer 14 is disposed directly against a ball limiting metallurgy (BLM)." Examiner disagrees. Note that Fig. 1 of the instant invention shows that the resin layer is disposed on the two layers of polyimide layer, yet the instant invention recites that "a resin film directly on the semiconductor chip." Therefore, Examiner assumes that "disposed directly on" does not necessarily imply "a direct contact with." With this understanding, Fig. 4 of Milewski clearly shows that a passivation layer 14 is disposed directly on the on the semiconductor chip having a direct contact and is disposed directly on the solder bumps 30 through a BLM layer.

Applicant argues that “Milewski does not suggest implementing relevant qualities (including the tin cap 37 and layer 14) of the devices together.” It is noted that the instant invention recites that “upper surfaces of said solder bumps protrude from said resin layer” not the eutectic solder (equivalent to the tin cap layer in Milewski’s) device protruding from the resin layer. And Fig. 4 of Milewski is based on the structure in Fig. 3 Prior art. Therefore, it is obvious that the resin layer applied for the Prior art would be applied in the same manner for the Milewski’s invention, resulting in a solder surfaces of the solder bumps protruded from the resin layer.

Applicant argues that “The references also fail to show or suggest ‘a plurality of lands formed on the mounting board.’ The lands 53 of Milewski are simply portions of the circuit card 21 and not ‘formed on’ the circuit card. In a natural interpretation of Milewski with respect to the present claims, the pads 51 would be compared to the presently claimed, ‘lands’ and the lands 53 would be a land portion (See present claim 31) of the mounting board.” This is a confusing statement. This argument merely shows that there is a mislabeling, however, also confirms that a plurality of lands is indeed formed on the mounting board.

Applicant argues that Milewski *teaches away* from implementing a precoated land and a coated solder ball together.” Col. 5, lines 1-40 of Milewski clearly shows implementing a precoated land and a coated solder ball together through disclosing a process of connecting the solder ball with a eutectic solder layer on the upper surface to the land/pad precoated with an oxidation inhibitor oxidation inhibitor (col. 1, lines 1-5) or Pb/Sn electroplated (col. 5, lines 39-41).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

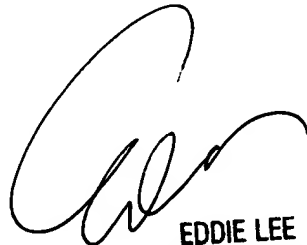
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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